In The Claims:

Please amend the Claims as follows:

1. (Currently Amended) A reference voltage generating circuit, comprising:

a distributing unit which generates via an output terminal a reference voltage, which has a lower voltage level than that of an external power supply voltage and varies according to an operating mode, in response to the external power supply voltage, the distributing unit having an enabling switch with a control terminal connected to the external power supply voltage;

a clamping control unit connected between the output terminal and a ground voltage, the clamping control unit for clamping a voltage level of the reference voltage at a constant level in response to a control voltage having a voltage level which is lower than that of the reference voltage; and

a control unit connected to the distributing unit for increasing or decreasing a voltage level of the reference voltage in response to first and second operating mode signals by controlling the operating mode of the distributing unit.

2. (Currently Amended) The circuit of claim 1, wherein the distributing unit comprises:

a first resistor connected between the external power supply voltage and the output terminal;

a second resistor connected between the output terminal and a first node from which the control voltage is output; and

first through fourth transistors connected in series between the first node and the ground voltage,

wherein the ~~gates~~ control terminals of the first through third transistors are connected to the output terminal,

and wherein the external power supply voltage is applied to the ~~gate~~ control terminal of the fourth transistor.

3. (Original) The circuit of claim 2, wherein the first through fourth transistors are NMOS transistors.

4. (Original) The circuit of claim 2, wherein the voltage level of the reference voltage is controlled by controlling a width-to-length ratio of each of the first through fourth transistors.

5. (Original) The circuit of claim 2, wherein the control unit comprises:

a first control transistor which is turned on or turned off in response to the first operating mode signal to increase or decrease the reference voltage level; and

a second control transistor which is turned on or turned off in response to the second operating mode signal to increase or decrease the reference voltage

level.

6. (Original) The circuit of claim 5, wherein the first control transistor is an NMOS transistor, and the source and the drain of the NMOS transistor are connected to the source and the drain of the first transistor and the first operating mode signal is applied to the gate of the NMOS transistor.

7. (Original) The circuit of claim 5, wherein the second control transistor is an NMOS transistor, and the source and the drain of the NMOS transistor are connected to the source and the drain of the third transistor and the second operating mode signal is applied to the gate of the NMOS transistor.

8. (Original) The circuit of claim 1, wherein the clamping control unit is a PMOS transistor, and the first and second ends of the PMOS transistor are connected to the output terminal and the ground voltage, respectively, and the control voltage is applied to the gate of the PMOS transistor.

9. (Original) The circuit of claim 1, wherein the first and second operating mode signals are mode register set ("MRS") signals.

10. (Currently Amended) ~~The circuit of claim 1~~ A reference voltage generating circuit, comprising:

a distributing unit which generates via an output terminal a reference voltage, which has a lower voltage level than that of an external power supply voltage and varies according to an operating mode, in response to the external power supply voltage;

a clamping control unit connected between the output terminal and a ground voltage, the clamping control unit for clamping a voltage level of the reference voltage at a constant level in response to a control voltage having a voltage level which is lower than that of the reference voltage; and

a control unit connected to the distributing unit for increasing or decreasing a voltage level of the reference voltage in response to first and second operating mode signals by controlling the operating mode of the distributing unit, wherein:

in a low operating frequency range, the first and second operating mode signals are at a first level;

in a high operating frequency range, the first and second operating mode signals are at a second level; and

in an intermediate frequency range, one of the first and second operating mode signals is at the first level and the other is at the second level.

11-27. (Canceled)

28. (New) A voltage generating circuit comprising:

mode means for controlling a voltage level of at least one of a first, a second and a third voltage in response to at least one operating mode signal;

comparison means for comparing the voltage level of the first voltage with the voltage level of the second voltage; and

adjusting means for controlling the voltage level of the third voltage in response to at least one of the mode means and the comparison means.

29. (New) A circuit as defined in Claim 28 wherein:

the mode means comprises a control unit;

the comparison means comprises a distributing unit; and

the adjusting means comprises a clamping control unit.

30. (New) A circuit as defined in Claim 28 wherein:

the mode means comprises a control unit;

the comparison means comprises a differential amplifier unit; and

the adjusting means comprises a distributing unit.

31. (New) A circuit as defined in Claim 28 wherein:

the mode means comprises a voltage level detecting unit;

the comparison means comprises the voltage level detecting unit; and

the adjusting means comprises a boosting unit.